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EXAMINER

UMEZ ERONINI, LYNETTE T

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/845,480

Applicant(s)

QUEK ET AL.

Examiner

Lynette T. Umez-Eronini

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) ✓
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US 4,789,648) in view of Toshiaki (English translation of JP 10-112503 A) and further in view of Kudo (US 6,420,261) and Havemann (5,565,384).

As pertaining to the claims 1, 3, and 5, Chow teaches a method of forming dual damascene openings in the fabrication of an integrated circuit device. The method comprises:

providing metal lines covered by an insulating layer overlying a semiconductor substrate (column 2, line 67 – column 3, line 6 and Figure 2);

depositing a quartz insulation layer 5 (first inorganic dielectric) over substrate 2 (column 3, lines 15-16) and "although the preferred embodiment also makes use of sputtered quartz or composite $\text{Si}_3\text{N}_4/\text{SiO}_2$ for insulation layers 5 and 8, other insulation materials, such as spin-on polyimides (same as organic dielectric layer) are also suitable," which reads on depositing an organic dielectric layer overlying said insulating layer;

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depositing a second insulation 8 of quartz or a composite $\text{Si}_3\text{N}_4/\text{SiO}_2$ layer over the structure as shown in **FIG. 2** (column 3, lines 24-27) and " (column 4, lines 24-27) reads on depositing an inorganic dielectric layer overlying said organic dielectric layer;

simultaneous formation of a stud via connection through an intervening insulator which comprises a first insulator (same as applicant's organic dielectric) layer, an etch stop layer, and a second insulator (same as applicant's inorganic dielectric) layer to an underlying patterned metallization (column 4, lines 40-44), reads on,

etching a via pattern into said inorganic dielectric layer;

etching said via pattern into said organic dielectric layer;

The channels (trench) and via holes etched into the second (same as applicant's inorganic dielectric) and first (same as applicant's organic) layers of insulation, respectively, are overfilled with metallization and excess metallization is removed by etching or by chemical-mechanical polishing (column 2, lines 42-47 and Figures 4-6) reads on,

thereafter etching a trench pattern into said second inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

Chow differs in failing to teach wherein no etch stop layer is formed between said organic dielectric layer and said organic dielectric, in **claim 1**.

Toshiaki teaches a damascene structure which lacks an etch stop layer between the organic dielectric layer and inorganic dielectric layer ([0013, lines 1,2] and Figure 3).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by forming a damascene structure which lacks an etch stop layer between the organic dielectric layer and inorganic dielectric layer for the purpose of reducing the cost in manufacturing a semiconductor device [0004, lines 6-7].

Chow in view of Toshiaki differs in failing to teach using patterned said inorganic dielectric layer as a mask, **in claim 1**.

Kudo teaches using an inorganic insulating film as a mask (column 14, lines 34-41).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki by using an inorganic dielectric layer as a mask, which is taught by Kudo for the purpose of improving the reliability of the semiconductor device (Kudo, column 14, lines 62-65).

Chow in view of Toshiaki and Kudo differ in failing to teach wherein said organic dielectric layer acts as an etch stop, **in claim 1**.

Havemann teaches, "Without the organic-containing dielectric layer **22** acting as an etch stop, the etch through the relatively thick inorganic dielectric layer **24** generally would have created a large void extending down the side of conductor **18**. This void can not only cause mechanical problems, but also, if subsequently filled with metal,

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decrease the distance (and therefore increase the capacitance) between the conductor and its adjacent neighbor (column 4, lines 27-35).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki and Kudo by using Havemann's organic dielectric layer which act as an etch stop for the purpose of prevention of large void extending down the side of the conductor, which causes mechanical problems between the conductor and its adjacent neighbor (Havemann, column 4, lines 27-35).

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP 503 A), Kudo ('261) and Havemann ('384) as applied to claim 1 above, and further in view of Joshi et al. (US 5,955,781).

Chow in view of Toshiaki, Kudo, and Havemann differ in failing to teach forming gate electrodes and source and drain regions in and on said semiconductor substrate.

Joshi teaches a dual damascene structure that comprises forming gate electrodes and source and drain regions in and on said semiconductor substrate (column 7, lines 51-63).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki, Kudo, and Havemann by forming gate electrodes and source and drain regions in and on said semiconductor substrate as taught by Joshi for the purpose of preventing short-circuiting in the semiconductor device.

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4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view Toshiaki (JP 503 A), Kudo (US '261), and Havemann ('384) as applied to claim 1 above, and further in view of Wang et al. (US 6,020,269).

Chow in view of Toshiaki, Kudo, and Havemann differ in failing to teach said inorganic dielectric layer comprises one of the following: CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen doped FSG, Z3MS, XLX, and or hydrogen silsesquioxane HSQ.

Wang teaches, "... typically silicon dioxide ... may include ... fluorine doped silicon glass (FSG) ... or low k polymer materials (column 4, lines 16-22).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view Toshiaki, Kudo, and Havemann by replacing quartz (silicon dioxide) with FSG as taught Wang because both quartz and FSG are seen as equivalent: they are dielectric materials. Substitution of one for the other would have been obvious for the purpose of providing medium for depositing a conductive layer.

5. Claims 6, 8, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP '503 A).

As pertaining to claims 6, 8, and 10, Chow teaches a method of forming dual damascene openings in the fabrication of an integrated circuit device. The method comprises:

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providing metal lines covered by an insulating layer overlying a semiconductor substrate (column 2, line 67 – column 3, line 6 and Figure 2);

depositing an organic dielectric layer overlying said insulating (5 and 8) layer (column 3, lines 15-16);

depositing an inorganic dielectric layer overlying said organic layer (column 3, lines 24-27; column 4, lines 24-27; and FIG. 2).

Chow further teaches, "The channels (trench) and via holes etched into the second (same as applicant's inorganic dielectric layer) and first (same as applicant's organic dielectric) layers of insulation, respectively, are overfilled with metallization. The excess metallization, on top of the second layer of insulation but not in the channels or via holes is removed by etching or by chem-mech (chemical-mechanical) polishing" (column 2, lines 42-43), which reads on,

etching a trench pattern into said inorganic dielectric layer; and

thereafter etching a via pattern through said inorganic dielectric layer and said organic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

Chow differs in failing to teach wherein no etch stop layer is formed between said organic dielectric layer and said organic dielectric, in **claim 6**.

Toshiaki teaches a damascene structure which lacks an etch stop layer between the organic dielectric layer and inorganic dielectric layer ([0013, lines 1,2] and Figure 3).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by forming a

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damascene structure which lacks an etch stop layer between the organic dielectric layer and inorganic dielectric layer for the purpose of reducing the cost in manufacturing a semiconductor device [0004, lines 6-7].

Chow differs in failing to teach etching a via pattern into said organic dielectric layer through said trench pattern.

Toshiaki teaches, "The silicon dioxide film 4 is selectively etched and an opening, in the form of a wiring pattern (same as applicant's trench) is formed. Then, the organic low dielectric constant film 3, and the silicon oxide film 2 in the opening 6 are sequentially and selectively etched, and a via hole 8 is formed" (Abstract).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by using Toshiaki's method of forming a via pattern into an organic dielectric layer through a trench pattern for the purpose of using an organic low dielectric constant film in a damascene process in the manufacturing of a semiconductor device, which can easily form a wiring embedded in the hole and the wiring slot, without increasing the number of processes (processing steps), (Toshiaki, [0006]).

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP 503 A) as applied to claim 6 above, and further in view of Joshi et al. (US 5,955,781).

Chow in view of Toshiaki differs in failing to teach forming gate electrodes and source and drain regions in and on said semiconductor substrate.

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Joshi teaches a dual damascene structure that comprises forming gate electrodes and source and drain regions in and on said semiconductor substrate (column 7, lines 51-63).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki by forming gate electrodes and source and drain regions in and on said semiconductor substrate as taught by Joshi for the purpose of preventing short-circuiting in the semiconductor device.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view Toshiaki (JP '503 A) as applied to claim 6 above, and further in view of Wang et al. (US 6,020,269).

Chow in view of Toshiaki differs in failing to teach said inorganic dielectric layers.

Wang teaches, "... typically silicon dioxide ... may include ... fluorine doped silicon glass (FSG) ... or low k polymer materials (column 4, lines 16-22).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view Toshiaki by replacing quartz (silicon dioxide) with FSG as taught Wang because both quartz and FSG are seen as equivalent: they are dielectric materials. Substitution of one for the other would have been obvious for the purpose of providing medium for depositing a conductive layer.

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8. Claims 11, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki JP '530 A).

As pertaining to claims 11, 13, and 15, Chow teaches a method of forming dual damascene openings in the fabrication of an integrated circuit device (column 1, lines 10-16). The method comprises:

providing metal lines covered by an insulating layer overlying a semiconductor substrate (column 2, line 67 - column 3, line 6 and Figure 2);

depositing an organic dielectric layer overlying said insulating layer (column 3, lines 15-16);

depositing an inorganic dielectric layer overlying said organic layer (column 3, lines 24-27; column 4, lines 24-27; and **FIG. 2**).

etching a via pattern into said inorganic dielectric layer (claim 1, column 4, lines 40-44);

Chow further teaches the channels (trench) and via holes into the second (same as applicant's inorganic dielectric layer) and first (same as applicant's organic dielectric) layers of insulation, respectively, are overfilled with metallization (column 2, lines 42-43) and the excess metallization, on top of the second layer of insulation but not in the channels or via holes is removed by etching or by chem-mech (chemical-mechanical) polishing, reads on,

etching a via pattern into said inorganic dielectric layer.

Chow differs in failing to teach wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer, **in claim 11**.

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Toshiaki teaches a damascene structure which lacks an etch stop layer between the organic dielectric layer and inorganic dielectric layer ([0013, lines 1,2] and Figure 3).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by forming a damascene structure which lacks an etch stop layer between the organic dielectric layer and inorganic dielectric layer for the purpose of reducing the cost in manufacturing a semiconductor device [Toshiaki, 0004, lines 6-7].

Chow also differs in failing to teach simultaneously etching said via pattern into said organic dielectric layer and etching a trench pattern into said inorganic dielectric layer, **in claim 11**.

It is the examiner's position that since Chow teaches separate steps in forming a via and trench respectively in an organic dielectric and inorganic dielectric layer, then it would be obvious to perform both said steps simultaneously for the purpose of completing the damascene structure. The performance of two steps simultaneously, which have previously been performed in sequence was held to have been obvious. *In re Tatincloux* 108 USPQ 125 (CCPA 1955).

Chow also differs in failing to teach one etching recipe is used for said organic dielectric layer and a different etching recipes is used for said inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

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Toshiaki teaches, "... the opening 6 (same as trench) ... and "... the etching conditions at this time is given, ... C_2F_6 as etching gas ... [0014]. Next the organic low dielectric constant film 3 and silicon-oxide film 2 of a portion of the silicon-oxide film 4 are ... one by one by using the resist pattern 7 as a mask, for example using the dry etching system ... [of opening 6 (same as trench)]. Then, the resist pattern 7 is removed. Of this, as shown in drawing 7, the veer hole 8 (same as via) is formed. ... and CHF_3 as etching gas. ... " [0015]. The aforementioned reads on, using one etching recipe for said organic dielectric layer and a different etching recipe for said organic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by using Toshiaki's method of using one etching recipe for said organic dielectric layer and a different etching recipes is used for said inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device for the purpose of easily forming a hole (via) and wiring slot (trench) in a damascene process using fewer lithographic steps (Toshiaki, [0009]).

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP '503 A) as applied to claim 11 above, and further in view of Joshi et al. (US '781).

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Chow in view of Toshiaki differs in failing to teach forming gate electrodes and source and drain regions in and on said semiconductor substrate.

Joshi teaches a dual damascene structure that comprises forming gate electrodes and source and drain regions in and on said semiconductor substrate (column 7, lines 51-63).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki by forming gate electrodes and source and drain regions in and on said semiconductor substrate as taught by Joshi for the purpose of preventing short-circuiting in the semiconductor device.

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP '530 A) as applied to claim 11 above, and further in view of Wang (US '269).

Chow in view of Toshiaki differs in failing to teach said inorganic dielectric layer comprises CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen doped FSG, Z3MS, XLX, and or hydrogen silsesquioxane HSQ.

Wang teaches, "... typically silicon dioxide ... may include ... fluorine doped silicon glass (FSG) ... or low k polymer materials (column 4, lines 16-22).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki by replacing quartz (silicon dioxide) with FSG as taught Wang because both

quartz and FSG are seen as equivalent: they are dielectric materials. Substitution of one for the other would have been obvious for the purpose of providing medium for depositing a conductive layer.

11. Claims 16, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP '530 A) and further in view of Dennison et al. (5,651,855).

As pertaining to claims 16, 19, and 20, Chow teaches a method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate (column 2, line 67 – column 3, line 6 and Figure 2);

depositing an inorganic dielectric layer (5) overlying said insulating layer (column 3, lines 15-16); and

depositing an organic dielectric layer overlying said inorganic layer (column 4, lines 24-27).

Chow teaches simultaneous formation of a stud via connection through an intervening insulator which comprises a first insulator (same as applicant's inorganic dielectric) layer, an etch stop layer, and a second insulator (same as applicant's organic dielectric) layer to an underlying patterned metallization (claim 1), reads on,

etching a via pattern into said organic dielectric layer.

Chow differs in failing to teach wherein no etch stop layer is formed between said inorganic dielectric layer and said organic dielectric layer; and thereafter etching a

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trench pattern into said organic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device, **in claim 16**.

Toshiaki teaches a damascene structure, which is shown to comprise a stacked silicon-oxide film **2**, an organic low dielectric constant film **3**, and silicon oxide film **4** layers form on a substrate **1** and which lacks an etch stop layer between the organic dielectric layer and inorganic dielectric layer ([0011, lines 2-3], [0012, lines 1-3], [0013, lines 1,2] and Figure 3). The said layers are etched to via hole **8** [0005, lines 1-4 and Figure 7] and the organic low dielectric constant film **3** is etched into the wiring slot (trench) **9** by using the silicon-oxide film **4** as a mask [0015, lines 1-3 Figure 8]. Wiring material is formed in hole **8** and wiring slot **9** and is ground (polished) by a CMP method [0017 and Figures 9 and 10]. The aforementioned further reads on,

etching via pattern into said organic dielectric layer; and thereafter etching a trench pattern into said organic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by forming a damascene structure which lacks an etch stop layer between the organic dielectric layer and inorganic dielectric layer and etching via and trench as taught by Toshiaki for the purpose of reducing the cost in manufacturing a semiconductor device [Toshiaki, 0004, lines 6-7].

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Chow in view of Toshiaki differs in failing to teach wherein said inorganic dielectric layer acts as an etch stop, **in claim 16**.

Dennison teaches, "The etch stop layer **16** of either silicon nitride, titanium oxide, aluminum oxide or other equivalent dense inorganic insulating material will be quite suitable to serve as an etch mask during the etching of the insulating layer **14** . . . (column 3, lines 46-50), which provides evidence that an inorganic dielectric layer acts as an etch stop.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki by using Dennison's inorganic dielectric layer that acts as an etch stop for the purpose of serving as an etching mask during etching of an underlying insulating layer (column 3, lines 46-50).

12. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP '503 A) in view of Dennison (US '855) as applied to claim 16 above, and further in view of Joshi (US '781).

Chow in view of Toshiaki and Dennison differ in failing to teach forming gate electrodes and source and drain regions in and on said semiconductor substrate.

Joshi teaches a dual damascene structure that comprises forming gate electrodes and source and drain regions in and on said semiconductor substrate wherein metal lines overlie and contact said semiconductor device structure (column 7, lines 51-63).

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It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki and Dennison by forming gate electrodes and source and drain regions in and on said semiconductor substrate wherein metal lines overlie and contact said semiconductor device structure, as taught by Joshi for the purpose of preventing short-circuiting in the semiconductor device.

13. Claim 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP '530A) and Dennison ('855) as applied to claim 16 above, and further in view of Wang (US '269).

Chow in view of Toshiaki and Dennison differ in failing to teach said inorganic dielectric layer as recited in the instant claim.

Wang teaches, "... typically silicon dioxide ... may include ... fluorine doped silicon glass (FSG) ... or low k polymer materials (column 4, lines 16-22).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki and Dennison by replacing quartz (silicon dioxide) with FSG as taught Wang because both quartz and FSG are seen as equivalent: they are dielectric materials. Substitution of one for the other would have been obvious for the purpose of providing medium for depositing a conductive layer.

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14. Claims 21, 24, 25, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP '530 A).

As pertaining to claims 21, 24, and 25, Chow teaches a method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate (column 2, line 67 – column 3, line 6 and Figure 2);

depositing a quartz insulation layer 5 (same as organic dielectric) over substrate 2 (column 3, lines 15-16) and “although the preferred embodiment also makes use of sputtered quartz or composite $\text{Si}_3\text{N}_4/\text{SiO}_2$ for insulation layers 5 and 8, other insulation materials, such as spin-on polyimides” (same as material as organic dielectric layer) are also suitable (column 4, lines 24-27), which suggests that insulation layers 5 and 8 are used interchangeably and respectively as inorganic and organic dielectric layers and reads on,

depositing an inorganic dielectric layer (5) overlying said insulating layer; and

depositing an organic dielectric layer overlying said inorganic layer.

Chow teaches simultaneous formation of a stud via connection through an intervening insulator which comprises a first insulator (same as applicant's inorganic dielectric) layer, an etch stop layer, and a second insulator (same as applicant's organic dielectric) layer to an underlying patterned metallization (claim 1), reads on,

etching a via pattern into said organic dielectric layer.

Chow differs in failing to teach wherein no etch stop layer is formed between said inorganic dielectric layer and said organic dielectric layer, **in claim 21**.

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Toshiaki teaches a damascene structure, which is shown to comprise a stacked silicon-oxide film **2**, an organic low dielectric constant film **3**, and silicon oxide film **4** layers form on a substrate **1** ([0011, lines 2-3], [0012, lines 1-3], [0013, lines 1,2] and Figure 3), which reads on, no etch stop layer between the organic dielectric layer and inorganic dielectric layer.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by forming a damascene structure which lacks an etch stop layer between the organic dielectric layer and inorganic dielectric layer and etching via and trench as taught by Toshiaki for the purpose of reducing the cost in manufacturing a semiconductor device [0004, lines 6-7].

Chow differs in failing to teach thereafter etching a via pattern into said organic dielectric layer through said trench pattern to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device, **in claim 21**.

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Toshiaki further teaches, the said layers (silicon-oxide film 2, an organic low dielectric constant film 3, and silicon oxide film 4) are etched to via hole 8 [0005, lines 1-4 and Figures 6, 7, and 8] and the organic low dielectric constant film 3 is etched into the wiring slot (trench) 9 by using the silicon-oxide film 4 as a mask [0015, lines 1-3 Figure 8]. Wiring material is formed in hole 8 and wiring slot 9 and is ground (polished) by a CMP method [0017 and Figures 9 and 10]. The aforementioned reads on,

thereafter etching a via pattern into said inorganic dielectric layer through said trench pattern to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device, **in claim 21**.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by etching a via pattern into said inorganic dielectric layer through said trench pattern as taught by Toshiaki for the purpose of reducing the cost in manufacturing a semiconductor device [0004, lines 6-7].

15. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP '503 A) as applied to claim 21 above, and further in view of Joshi (US '781).

Chow in view of Toshiaki differs in failing to teach forming gate electrodes and source and drain regions in and on said semiconductor substrate.

Joshi teaches a dual damascene structure that comprises forming gate electrodes and source and drain regions in and on said semiconductor substrate

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wherein metal lines overlie and contact said semiconductor device structure (column 7, lines 51-63).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki by forming gate electrodes and source and drain regions in and on said semiconductor substrate wherein metal lines overlie and contact said semiconductor device structure, as taught by Joshi for the purpose of preventing short-circuiting in the semiconductor device.

16. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP '530 A) as applied to claim 21 above, and further in view of Wang (US 269).

Chow in view of Toshiaki differs in failing to teach said inorganic dielectric layer as recited in the instant claim.

Wang teaches, "... typically silicon dioxide ... may include ... fluorine doped silicon glass (FSG) ... or low k polymer materials (column 4, lines 16-22).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki by replacing quartz (silicon dioxide) with FSG as taught Wang because both quartz and FSG are seen as equivalent: they are dielectric materials. Substitution of one for the other would have been obvious for the purpose of providing medium for depositing a conductive layer.

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17. Claims 26 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '629) in view of Toshiaka (JP '530 A).

Chow teaches a method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate (column 2, line 67 – column 3, line 6 and Figure 2);

depositing an inorganic dielectric layer (5) overlying said insulating layer (column 3, lines 15-16); and

depositing an organic dielectric layer overlying said inorganic layer (column 4, lines 24-27).

Chow teaches simultaneous formation of a stud via connection through an intervening insulator which comprises a first insulator (same as applicant's inorganic dielectric) layer, an etch stop layer, and a second insulator (same as applicant's organic dielectric) layer to an underlying patterned metallization (claim 1), reads on,

etching a via pattern into said organic dielectric layer.

Chow differs in failing to teach where in no etch stop layer is formed between said organic dielectric layer and said organic dielectric.

Toshiaki teaches a damascene structure which lacks an etch stop layer between the organic dielectric layer and inorganic dielectric layer ([0013, lines 1,2] and Figure 3).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by forming a damascene structure which lacks an etch stop layer between the organic dielectric layer

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and inorganic dielectric layer for the purpose of reducing the cost in manufacturing a semiconductor device [0004, lines 6-7].

Chow also differs in failing to teach simultaneously etching said via pattern into said inorganic dielectric layer and etching a trench pattern into said organic dielectric layer.

It is the examiner's position that since Chow teaches separate steps in forming a via and trench respectively in an inorganic dielectric and organic dielectric layer, which reads on etching a via pattern into said inorganic dielectric layer and etching a trench pattern into said organic dielectric layer, then it would be obvious to perform both said steps simultaneously for the purpose of completing the damascene structure. The performance of two steps simultaneously, which have previously been performed in sequence was held to have been obvious. *In re Tatincloux* 108 USPQ 125 (CCPA 1955).

Chow further differs in failing to teach one etching recipe is used for said organic dielectric layer and a different etching recipes is used for said inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

Toshiaki teaches, "... the opening 6 (same as trench) ... and "... the etching conditions at this time is given, "... C_2F_6 as etching gas ... [0014]. Next the organic low dielectric constant film 3 and silicon-oxide film 2 of a portion of the silicon-oxide film 4 are ... one by one by using the resist pattern 7 as a mask, for example using the dry

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etching system . . . [of opening 6 (same as trench)]. Then, the resist pattern 7 is removed. Of this, as shown in drawing 7, the veer hole 8 (same as via) is formed. . . . and CHF_3 as etching gas. . . ." [0015]. The aforementioned reads on, using one etching recipe for said organic dielectric layer and a different etching recipe for said organic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow by using Toshiaki's method of using one etching recipe for said organic dielectric layer and a different etching recipes is used for said inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device for the purpose of easily forming a hole (via) and wiring slot (trench) in a damascene process using fewer lithographic steps (Toshiaki, [0009]).

18. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP 503 A) as applied to claim 26 above, and further in view of Joshi (US '781).

Chow in view of Toshiaki differs in failing to teach forming gate electrodes and source and drain regions in and on said semiconductor substrate.

Joshi teaches a dual damascene structure that comprises forming gate electrodes and source and drain regions in and on said semiconductor substrate

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wherein metal lines overlie and contact said semiconductor device structure (column 7, lines 51-63).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki by forming gate electrodes and source and drain regions in and on said semiconductor substrate wherein metal lines overlie and contact said semiconductor device structure, as taught by Joshi for the purpose of preventing short-circuiting in the semiconductor device.

19. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US '648) in view of Toshiaki (JP '530 A) as applied to claim 26 above, and further in view of Wang (US 269).

Chow in view of Toshiaki differs in failing to teach said inorganic dielectric layer as recited in the instant claim.

Wang teaches, "... typically silicon dioxide ... may include ... fluorine doped silicon glass (FSG) ... or low k polymer materials (column 4, lines 16-22).

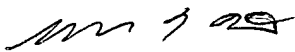
It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Chow in view of Toshiaki by replacing quartz (silicon dioxide) with FSG as taught Wang because both quartz and FSG are seen as equivalent: they are dielectric materials. Substitution of one for the other would have been obvious for the purpose of providing medium for depositing a conductive layer.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 703-306-9074. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703-308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

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June 12, 2003


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